DESIGN OF UNIVERSAL GATES USING MATLAB & MICROWIND

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ABSTRACT

According to Moore's Law, the no of transistors in an IC chip doubles every 18 months. This leads in increase in power density. Hence in modern power circuits, the main factor of the circuit efficiency is power efficiency. Due to scaling, leakage power accounts for an increasingly large portion of the total power consumption in deep submicron technologies. In this article, we proposed a methodology to find the problems occurring while scaling it into small size with some factor. We have simulated the inverter circuit using CMOS in MATLAB, DSCH3 .where we can vary the physical dimensions of the MOSFET. The outputs were observed and the time delay was calculated. The above results showed that, as we go on reducing the size, the performance enhances. Due to some limitations, the CMOS were facing some of the problems like Drain induced barrier lowering (DIBL), Velocity Saturation, Punch through, Oxide Breakdown, Channel length modulation.Hence due to the above factors, FinFET technology has proposed as an alternative to deep submicron bulk CMOS. FinFET is likely to meet the performance requirements in the sub-20nm gate length regime. FinFET will replace the traditional MOSFET due to its better performance in sub 20nm regime and also it has excellent control over the problems faced by the Traditional CMOS.The objective is to simulate the inverter circuit using CMOS through MATLAB,. The merits of small scale are also discussed. The future work is to replace the Bulk-CMOS with the nano-CMOS and make the system faster. This includes SD-RAM, Processor, logic circuits, and switches, and also where we can implement these applications. FinFET being one of the nano device is the better option among all the devices because of smaller size among all the above. FinFET can overcome all the Problems caused by scaling the MOSFET into the nano regime.Wide FinFET devices are built utilizing multiple parallel fins between the source and drain. Independent gating of the FinFETs double gates allows significant reduction in leakage current.

KEYWORDS: CMOS, Drain Gate, Source, MATLAB